Technical Field of Invention

This invention relates to the field of charge coupled and active pixel image sensors that are fabricated in the III-V material systems and have sensitivities over a broad spectral range including the UV, visible, near and far infrared regions.

A III-V Charge Coupled Device Suitable for Visible, Near and Far Infra-Red Detection

BACKGROUND OF INVENTION

Next generation imaging systems are required to have Charged Coupled Devices (CCD's) that operate at very high frequencies and to have a high resistance to radiation flux (the imager is said to be radiation hardened). Many of these applications are in space where radiation flux is significant and reliability is critical. State-of-the-art imagers are constructed as Si integrated circuits in the form of CCD's or active pixel arrays. In the CCD, the pixels are clocked sequentially to a common output amplifier. In the active pixel array, the array is x-y addressable and each pixel is output to its own dedicated amplifier (the array is output on a row by row or column by column basis).

Si technology is limited by the presence of the silicon oxide in both the active and passive regions of the integrated circuit in a number of ways. A main limitation is the sensitivity of the oxide to radiation flux. The radiation creates traps and other charged defects in the insulator which alter the internal voltage thresholds in both active and passive regions within the integrated circuit. After a certain cumulative exposure level, these threshold changes render the circuit inoperable. The gate oxide creates limitations in other ways as well. The Si CCD couples one pixel to the other via overlapping gates. Each overlapping gate creates a small region of thicker oxide between pixels which inhibits charge transfer and therefore sets a speed limitation upon the CCD. These oxide barriers are fundamental to the Si CCD and constitute a transfer speed limitation. Some approaches have been employed to eliminate these effects such as the virtual phase CCD. However, these structures are then faced with barriers created by implant misalignment and a lack of well capacity. In any event the transfer speed in the Si CCD rarely exceeds a few MHz.

A further limitation of the Si CCD is its spectral sensitivity. The Si CCD absorbs radiation across its energy gap and therefore is insensitive to radiation with a wavelength longer than about 1um. It is also insensitive to UV radiation

III-V device structures based upon GaAs substrates have the potential to overcome the above limitations. In particular, the GaAs CCD has the potential to absorb within a quantum well between the various subbands. This provides the GaAs device with unique capabilities of intersubband absorption and sensitivity in the mid wavelength infrared, long wavelength infrared and very long wavelength infrared regions. The GaAs device structures that currently perform the intersubband detector functions are the QWIP

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(quantum well infrared photodetector) devices. Two significant limitations of the QWIP as currently implemented are the existence of a significant level of dark current that neccesitates cooling of the device to 77K and the fact that the device is not compatible with GaAs integrated circuits. When originally demonstrated the QWIP was considered advantageous because of its potential compatibility with GaAs integrated circuits. However, this compatibility has never been established and so present technology combines the GaAs QWIP wafer in a hybrid fashion with a Si read-out integrated circuit. There have been several efforts to build CCD shift registers using the basic transistor structures of the MESFET and HEMT devices. These technologies have always been plagued by the problem of low transfer efficiencies between pixels in the array. The proposed solutions have been to utilize a resistive coupling between pixels, which would provide drift aided transfer. The problem has been that no viable technique to implement resistive coupling has been found . The use of deposited resistive layers was attempted but the resistive control problems discouraged further investigations.

It is an object of this invention to provide a CCD technology in a III-V semiconductor system which is capable of very high transfer rates, substantially improved maximum charge compared to Si technology, and substantially improved radiation hardness properties compared to Si technology. This CCD technology will implement the resistive coupling structure in a natural way via the crystal growth which optimizes the charge transfer efficiency.

It is another object of this invention to provide a CCD technology which may absorb radiation in the broad range from 3um –20um via the intersubband absorption

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mechanism and convert the radiation to packets of charge for transfer to the CCD output amplifiers

It is another object of this invention to provide a CCD technology which has optical sensitivity in the uv, visible and near IR portions of the electromagnetic spectrum

It is another object of this invention to implement the CCD in an integrated fashion together with HFET technology such that analog to digital conversions can be made on the data.

It is another object of this invention to implement the CCD as part of a monolithic optoelectronic integrated circuit such that a vertical cavity surface emitting laser is available at the output amplifier of the CCD to facilitate the coupling of digital data from the chip into an optical fiber for transmission.

It is a final object of this invention to implement an active pixel within a III-V optoelectronic technology which is sensitive by bandgap absorption in the uv, visible, and near IR portions of the spectrum and sensitive by intersubband absorption in the MWIR and LWIR

SUMMARY OF THE INVENTION

A CCD epitaxial growth structure and fabrication technology have been invented which utilize a modulation doped interface to create an inversion channel for the storage of charge packets. The charge transfer is facilitated by the unique features of the epitaxial growth which include two delta-doped sheets of p type doping. One p type sheet is very close to the inversion channel and enables a resistive coupling between adjacent

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wells through a very thin sheet of highly doped material. The resistive coupling enables a high field and optimized drift velocity between pixels during the transfer phase which is responsible for the very high transfer rate. The second charge sheet positioned at the wafer surface enables a very low resistance ohmic contact to the gate metal contact. It is this ohmic contact that enables the HFET, which is the fundamental field effect device in the technology

The inversion channel is comprised of 2 or 3 quantum wells and these quantum wells may absorb incident radiation in the MWIR and LWIR regions. The CCD is unique because the absorption of radiation is used to empty the quantum well and the charge leaving the well, flows as recombination current to the gate ohmic contact. Therefore for the sensing of signals by the intersubband absorption mechanism in this invention, the imaged signal is formed as the depletion of an initially full well of charge and this depleted condition is clocked to the output node. On the other hand, the CCD may also image signals in the UV, the visible and the near IR regions of the spectrum by conventional band gap absorption

The device is described in the embodiment of the inversion channel technology which is a generalized approach to the implementation of optoelectronic devices as integrated components based upon the use of modulation doped structures. As such, the embodiment enables lasers and optical switches as well as the CCD to be implemented. In this description of the invention, a refractory emitter or gate metal contact is used for the transfer portion of the pixel. Also, dielectrics are used above the gate to form ¼ wavelength pairs for the imaging portion of the pixel. These dielectrics, when taken together with an epitaxially grown mirror below the active device structure constitute a

resonant cavity at the wavelength of interest in the LWIR or MWIR regions. In the

described embodiment, ion implants are used for several purposes. The N type implant is

used to form source and drain regions to the inversion channel, and it is also used to shift

the threshold voltage of the inversion channel interface. The epitaxial structure is grown

as a normally off (enhancement) device and then the N type implant is used to create

regions of normally on (depletion) devices and it is these regions where the charge

packets are stored. Oxygen implants may also be used to create high resistance regions

below the implants. The technology utilizes the oxidation of AlAs and other layers with

large aluminum percentages to achieve passivation, isolation and dielectric mirrors below

the structure.

The basic structure of the pixel and the output amplifiers which are employed in

the CCD may also be used to design an active pixel sensor. In such a design, each pixel

is interfaced to an output amplifier and a row or a column is output in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a schematic view of the epitaxial layer structure indicating the modulation doped

interface, the delta-doped resistively coupled layer and the delta-doped p contact layer

FIG.2 is a fabricated device cross-section of the CCD pixels including the pixel storage

region, the pixel blocking region and the inter-pixel transfer region.

FIG.3 is an energy diagram cross-section in the vertical direction through a storage pixel in the illuminated condition showing all of the significant current flows from the contacts and into and out of the well.

FIG.4 is schematic drwaing of the last storage well in the CCD and its connection by way of a separate clocked output gate to the output differential amplifier by way of a floating diffusion node which is reset each clock cycle. For the active pixel, V_ϕ is the single storage element connected to the output stage.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG.1 shows the epitaxial layer structure corresponding to the preferred embodiment and from which the CCD, the active pixel and the HFET can be made. The layer structure starts from a semi-insulating GaAs substrate 100 and grows a DBR mirror stack of 1 - 3 pairs of ¼ wavelength mirror using combinations of GaAs as layer 151 and AlAs as layers 152 which are subsequently oxidized to produce layers of Al_xO_y positioned between layers of GaAs. These layers form a bottom mirror for a cavity which is resonant at the intersubband wavelength of interest. Only a few pairs are used (1 - 3) to create a modest resonance in order to limit the total layer thickness and therefore epitaxial growth time. Following the DBR growth, a layer 170 of p+ GaAs of about 0.5μm is grown to enable a bottom ohmic contact to the collector . Then a layer 171 of $Al_{x1}Ga_{y1}As$ (1<x1<0.4) is grown to a thickness of about 1000-2000Å to assist in the contact formation with a p type doping of about $10^{18} cm^{-3}$ .and is followed by another layer 156 of undoped $Al_{x1}Ga_{y1}As$ of about 1000-3000 Å to provide carrier confinement.

This is followed by layer 157 of undoped $Al_{x2}Ga_{y2}As$ (0.3<y1<0.1) and then a separation layer 158 of undoped GaAs. Layer 158 enables a growth interruption to lower the growth temperature for growing the quantum well(s). Layers 157 and 158 isolate the quantum wells from the carrier confinement layers 156. Next the undoped quantum well 160 and and undoped barrier layer 159 are grown as a pair and there may be one to three pairs. The quantum well has been designed for intersubband absorption. A thin layer 161 of undoped GaAs of about 30 Å is then grown as a spacer which enables a growth temperature change between the InGaAs well and the layers above the well(s). The GaAs spacer is followed by an undoped spacer layer 162 of about 30 Å of $Al_{x2}Ga_{y2}As$. Then the modulation doped layer 163 of N+ type doped $Al_{x2}Ga_{y2}As$ is grown with a thickness of 40-100Å to contain an ion density of $10^{12}cm^{-2}<Q<4x10^{12}cm^{-2}$. On top of the modulation doped layer is grown an undoped capacitor spacer layer 164 of 100-300 Å thickness which can be as thin as possible consistent with the growth and fabrication. On top of the capacitor layer is grown a P+ doped layer 165 which serves as the charge source layer for the gate. This layer should be as thin as possible and as highly doped as possible providing that it remains only partially depleted under all conditions of operation, i.e. a portion of this layer, however small, always remains undepleted. Above the charge source layer is grown a cladding layer 166 of thickness 500 Å <z<2000 Å, of doping in the range of $10^{17}cm^{-3}$ and of composition $Al_{x1}Ga_{y1}As$. This layer serves to block minority carrier injection into the gate. The final layer 167 is a GaAs layer of about 100 Å or thinner and with P+ type doping which enables the formation of a very low resistance ohmic contact for hole carriers.

The CCD is formed as a series of mesas 115 in Fig.2 and referred to as pixels, separated by regions 116 referred to as the inter-electrode transfer regions in Fig.2 . The mesas are created by patterning the original wafer (with photoresist for example) and then etching (typically by reactive ion etching for accuracy) to the charge source layer. Between the electrodes, an ion implant 121 is positioned so that the storage region and the adjacent barrier region are connected by a high conductivity region. This implant 121 is simultaneously used to form the source and drain regions of all transistors in the integrated circuit. Thus each storage region is connected to the next barrier region by a source implant. These inter-electrode regions are designed to maximize the drift current from pixel to pixel during charge transfer. Suppose that the voltage difference between clock phases is 2V and it is desired to achieve the maximum channel velocity corresponding to $E=5\times10^3$ V/cm. Then an inter-electrode region width of 4μm would be desirable. The pixels are divided into a barrier region 117 and a storage region 118. The barrier region is contacted by the metal gate electrode 120 which is formed from a refractory metal such as tungsten or a tungsten alloy and produces an ohmic contact with the topmost GaAs layer 114. The gate electrode is formed upon the as-grown epitaxial material which has an enhancement threshold meaning that it is in the off condition with zero-gate voltage. The storage region is adjacent to the barrier region and is defined with an ion implant 119 of N type species into the active layer. Therefore, the region of the mesa without the implant, defines the barrier region. The purpose of the implant is to move the threshold of the interface to a normally on condition so that the potential profile under the gate electrode appears as shown in Fig.3. The metal emitter is patterned to be approximately positioned over the barrier portion and to be equal to or greater than

the barrier length. It is self-aligned to the left edge of the mesa. However, the P+ GaAs

layer 114 is low enough in resistance to force the entire surface of the mesa to be at the

potential of the metal electrode for all the current densities of interest in the operation.

The storage section of the pixel is therefore at a constant potential along its length y in

Fig.2 and this means the storage section is an equipotential region. The operation of this

CCD is 1 ½ phase which means that alternate electrodes are clocked to a voltage Vϕ and

the other electrodes are held at a dc potential V_{dc}. The potential profiles under the clocked

electrode and the dc electrode are shown in Fig.3, which illustrates the transfer

mechanism. The voltage difference $\Delta V = V\phi - V_{dc}$ is applied to the resistor consisting of

the P+ layer 112. The length of the resistor is chosen to maximize the velocity in the

interelectrode transfer region. The maximum velocity therefore maximizes the current

flow which is given by J=qvn, where v is the carrier velocity, q is the electronic charge

and n is the carrier density. To optimize the transfer efficiency, it is necessary to

maximize the current flow. This is achieved with the maximum value of v and the

maximum value of n. The maximum value of v is obtained as just discussed and the

maximum value of n is obtained by the implanted N+ region between electrodes as

discussed above.

The scheme just discussed is a 1 ½ phase clocking scheme. As is well known in Si

technology, there are many possible clocking schemes and these may also be

implemented here. These include a) a three phase clocking scheme, b)a fully two phase

clocking scheme, and c)a uni-phase clocking scheme. The uni-phase clocking scheme is

usually referred to as a virtual phase CCD and is achieved with a series of p and n

implants. The uni-phase operation has been exploited successfully in Si CCD's which use

a buried electron channel to store the charge. The surface of the buried channel is inverted by voltage to produce a hole inversion channel which clamps the potential of the electron channel. This natural clamping of the surface potential by the formation of a p channel eliminates the need for a separate dc electrode allowing a single electrode to be used. The voltage at which this clamping occurs is controlled locally with a p type implant. All of these clocking schemes are applicable to the Inversion Channel GaAs CCD.

The CCD described above has the unique capability of detecting an input signal in the spectral range from about 3µm to 20µm by the mechanism of intersubband absorption. The energy band diagram of the device is shown in Fig.3 . It shows the quantum well and the current flows of charge carriers which may either fill the well or empty the well. The current flows into the well are the thermal emission from the modulation doped layer 110 to the left of the well, and the generation currents flowing toward the well(s) from the collector depletion layer consisting of the layers 104, 105, 106, and 107 and from the quantum well(s) and barrier(s) which are layers 108 and 109 respectively. The currents flowing out of the well are the thermal emission current from the quantum well into the modulation doped layer 112 and the photocurrent from the quantum well into the modulation doped layer produced by the intersubband absorption in the quantum well. The other important current flow is the recombination current J_{rb} which allows electrons to flow from the modulation doped layer to the emitter contact via electron-hole recombination current in the capacitor layer 113. During the operation as a photodetector, the emitter is forward biased with respect to the collector. This means that the capacitor layer is forward biased and the collector layer is reverse biased which

enables the photocurrent to be conducted out of the system by forward bias and the dark current current flow in the system to be controlled by the reverse bias across the collector. The operation of the photodetector is described as follows. The quantum well is initially filled substantially in the absence of light. A reasonable design is that the Fermi energy is above the first subband in the quantum well. Then the absorption will be maximized because it is proportional to the number of electrons in the initial state. When long wavelength light is incident, then the photocurrent empties the quantum well. The dark current flowing into the well is produced by the generation current which is produced by emission across the energy gap of the quantum well or the barrier regions. The noise current i_n in the device which represents the limit to the detectable power is specified by the dark current I_d and it is

$$i_n^2 = 2qI_dB$$

where q is the electronic charge and B is the bandwidth. In a conventional QWIP device, the dark current flows over a small barrier of a size comparable to the quantum well and therefore to obtain high background limited operation , it is necessary to cool the device to cryogenic temperatures of 50-60K in order to reduce I_d. Only at these temperatures can the shot noise associated with the dark current be reduced to a level that is comparable to the noise associated with the black body radiation from the scene at a temperature of 300K.

The structure illustrated in Fig.3 has a fundamental advantage in reducing the dark current flow even at temperatures up to and above 300K. The reason is that the barrier to the generation of dark current and the barrier to the optical emission from the quantum well are distinctly different. As the diagram shows, the dark current is produced

by the thermal emission across the energy gap of either the quantum well (corresponding to strained InGaAs with a bandgap of about 1.24eV), the barrier region (corresponding to GaAs with a bandgap of 1.42eV), and the depletion regions (corresponding to Al$_{x2}$Ga$_{y2}$As with a bandgap of 1.65eV). Generally speaking the depletion regions become the main source of dark current. In contrast to the dark current barrier, the optical emission barrier is the energy interval between the first subband in the quantum well and the top of the well (this is basically the depth of the quantum well). Because this structure has decoupled the dark current generation barrier from the optical emission barrier, then it is possible to operate at room temperature and still achieve BLIP operation. Therefore we may realize all of the benefits of high resolution and high speed photovoltaic sensing offered by the QWIP detection mechanism with an uncooled semiconductor chip.

The infrared detection mechanism described above has been described as an integral part of an efficient CCD structure in GaAs. However the detector could equally as well be incorporated into the photo-sensitive portion of an active pixel structure. In the active pixel , the charge is transferred across one barrier to a bit line which connects to the sense amplifier. The charge transfer mechanisms are identical to those of the CCD, but the charge transfer efficiency is much less of an issue because there is only one transfer gate separating the storage area from the sensing node. The tradeoff is that the fill factor of the active pixel is less than the CCD because more circuitry is required. Therefore the operation of the intersubband detector is identical in the CCD and active pixel architectures.

In both the CCD and the active pixel devices, the signal of interest is actually the the charge that is removed from the well. For very weak optical input signals, very little charge is removed and for very strong optical inputs the well is essentially emptied at the end of the imaging cycle. The situation is ideal for the elimination of noise in the detection process because it requires differential operation to obtain the actual output signal. For example, if the output of the imaged pixel is input to one side of a differential amplifier, then it is appropriate to input a signal to the other side of the DA from a full well to perform as a reference level. These connections are illustrated in Fig.4 which shows a storage gate V_ϕ, a transfer gate V_{dc}, a reset gate V_{reset}, a differential amplifier and two reference nodes, one for a full well and one for an empty well. This situation is identical to that used in the correlated double sampling scheme in advanced CCD read-out circuits to reduce set:reset noise. There are several noise mechanisms contributing noise to the amplifier inputs which include clocking noise, kTC noise on the reset transistor, and shot noise on the dark current to mention a few. All of the noise mechanisms that are common to the read-out of the cell with and without data, are reduced by the common mode rejection ratio of the differential amplifier. Therefore the intersubband detection within the inversion channel has a fundamental advantage because the differential process is essential to recover the signal, and yet at the same time, it performs the role of reducing many noise mechanisms according to the differential rejection of common mode signals.

What is claimed is

1. A semiconductor imaging device comprised of the following layer structure: